(54) **Trench-gated power MOSFET with protective diode**

(57) A power MOSFET includes a trenched gate which defines a plurality of MOSFET cells. A protective diffusion is created, preferably in an inactive cell, so as to form a diode that is connected in parallel with the channel region in each of the MOSFET cells. The protective diffusion, which replaces the deep central diffusion taught in U.S. Patent No. 5,072,266, prevents impact ionization and the resulting generation of carriers near the corners of the gate trench, which can damage or rupture the gate oxide layer. Moreover, the diode can be designed to have a breakdown voltage which limits the strength of the electric field across the gate oxide layer. The elimination of a deep central diffusion permits an increase in cell density and improves the on-resistance of the MOSFET.

FIG. 3

Description

CROSS REFERENCE TO RELATED APPLICATION

5   This application is related to Application No. [Attorney Docket No. M-3260], filed concurrently herewith, which is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

10   This invention relates to power field-effect transistors and, in particular, to a metal-oxide-silicon field-effect transistor (MOSFET) in which the gate is positioned in a trench formed on the surface of the silicon.

BACKGROUND OF THE INVENTION

15   Trench-gated MOSFETs are a class of MOSFETs in which the gate is positioned in a trench that is formed at the surface and extends into the silicon. The gate is formed in lattice-like geometric pattern which defines individual cells of the MOSFET, the pattern normally taking the form of closed polygons (squares, hexagons, etc.) or a series of interdigitated stripes or rectangles. The current flows in vertical channels which are formed adjacent to the sides of the trenches. The trenches are filled with a conductive gate material, typically doped polysilicon, which is insulated from the
20   silicon by a dielectric layer normally consisting of silicon dioxide.

Two critical characteristics of a power MOSFET are its breakdown voltage, i.e., the voltage at which it begins to conduct current when in an off condition, and its on-resistance, i.e., its resistance to current flow when in an on condition. The on-resistance of a MOSFET generally varies directly with its cell density, since when there are more cells per unit area there is also a greater total "gate width" (around the perimeter of each cell) for the current to pass through. The
25   breakdown voltage of a MOSFET depends primarily on the doping concentrations and locations of the source, body and drain regions in each MOSFET cell.

The MOSFET is typically formed in a lightly-doped epitaxial layer of silicon which is grown on a heavily-doped silicon substrate. The gate trenches normally extend into the epitaxial layer and are frequently rectangular, with flat bottoms bounded by corners. This configuration creates a problem in that, when the MOSFET is turned off, the electric
30   field reaches a maximum near the corners of the gate trenches. This can lead to avalanche breakdown and impact ionization near the surface of the gate oxide, with the consequent generation of carriers. If the carriers are generated within a mean free path of the interface between the silicon and the gate oxide, they may have sufficient energy to pass through the interface and become injected into the gate oxide layer. Carriers that are able to surmount the silicon/silicon dioxide energy barrier are often referred to as "hot carriers." Hot carrier injection can ultimately damage the gate oxide
35   layer, causing changes in threshold voltage, transconductance or on-resistance, and thereby impair or destroy the MOSFET.

U.S. Patent No. 5,072,266 teaches a technique of suppressing voltage breakdown near the gate by the formation, in the MOSFET cell, of a deep central body diffusion that extends below the bottom of the trenches. This deep central diffusion shapes the electric field in such a way that breakdown occurs in the bulk silicon away from the gate, in a loca-
40   tion which prevents hot carriers from reaching the gate oxide layer. A cross-sectional view of a MOSFET in accordance with U.S. Patent 5,072,266 is shown in Fig. 1, which illustrates a MOSFET cell 10 containing a trenched gate 11, an N+ source region 12, an N+ substrate (drain) 13, an N-epitaxial layer 14, and a deep central P+ diffusion 15. Note that the lowest point of P+ diffusion 15 is below the bottom of gate 11.

The doping of deep P+ diffusion 15 is greater than the doping of P-body 16 in the region of the channel, designated
45   by the dashed line and reference numeral 17. As a result, the distance Y_S between the gate trenches must be maintained at or above a minimum value. Otherwise, the deep P+ dopant will diffuse into the channel 17 and raise the threshold voltage V_{tn} of the device. The value of Y_s, along with the thickness of the gate, defines the cell density and helps to determine the on-resistance of the MOSFET.

To fabricate an extremely low voltage, low on-resistance power MOSFET, the dimensions of the device are gener-
50   ally scaled down. In particular, the cell density is increased and the epitaxial layer is made thinner, even to the point that the gate trenches may extend into the heavily-doped substrate. Such a MOSFET is illustrated as MOSFET 20 in Fig. 2A.

This creates an entirely new set of design criteria. Referring to Fig. 2A, since the corners 21C of the gate trenches 21 are surrounded by the N+ substrate 13, the electric field at these locations drops entirely across the gate oxide layer.
55   While the formation of hot carriers in the silicon may be lower, the high electric field on the gate oxide layer may still lead to device degradation or damage. In one condition, when the gate is biased at essentially the same potential as the source and body (i.e., the device is turned off), a serious concern is that the gate oxide layer at the bottom of the trenches must support the entire voltage across the device. Compared to the embodiment of Fig. 1, there is no epitaxial layer to absorb a portion of this voltage difference.

An equivalent circuit for MOSFET 20 is shown in Fig. 28. Diode D_{DB} represents the PN junction between N-epitaxial layer 14 and P-body region 22, and capacitor C_{GD} represents the capacitor across the gate oxide layer 21A

SUMMARY OF THE INVENTION

The trench-gated MOSFET of this invention is formed in a semiconductor chip which includes a substrate alone or in combination with an overlying epitaxial layer. The gate of the MOSFET is formed in a trench which extends downward from the surface of the chip. The MOSFET includes a source region of a first conductivity type, a body region of a second conductivity type, and a drain region of the first conductivity type, which are arranged vertically along a side wall of the trench. The gate trenches may extend into the epitaxial layer, or through the epitaxial layer into the substrate.

The MOSFET is formed as a plurality of cells which are defined by the gate trench. The cells may be of any shape. For example, the cells may be in the form of a square or hexagon or a series of parallel stripes or rectangles.

In accordance with this invention, there is created in the chip a protective diffusion of the second conductivity type, which forms a PN junction with first conductivity material in the epitaxial layer or substrate. This PN junction functions as a diode. A metal layer ties the protective diffusion (i.e., one terminal of the diode) to the source regions of the MOSFET cells such that the diode is connected in parallel with the channels of the MOSFET cells.

In a preferred embodiment, the protective diffusion is formed in certain of the cells in a selected pattern across the MOSFET.

The protective diffusion of second conductivity type operates to reduce the strength of the electric field across the gate oxide and at the corners of the trenches and limits the formation of hot carriers in the vicinity of the trench, particularly in embodiments wherein the trenches extend into the epitaxial layer. The diode operates as a voltage clamp and thereby limits the voltage across the gate oxide layer, particularly in embodiments wherein the trenches extend into the substrate and the gate oxide must support the entire voltage drop across the MOSFET.

In a preferred embodiment, one cell containing a protective diffusion ("diode cell") is provided for a selected number of active MOSFET cells ("active cells"), in a repetitive pattern across the MOSFET. The number of diode cells per active cells is determined by the design criteria of the MOSFET. In general, for example, MOSFETs which are expected to experience breakdown more often will require a greater proportion of diode cells.

The presence of the diode cell also tends to carry a large portion of the drain-to-body diode current when the MOSFET is operated with its body diode forward-conducting. Such operation (called Quadrant III operation for an N-channel device) commonly occurs when an inductor or motor is driven by a push-pull or bridge-configured pair of MOSFETs. High diode currents in the active cells are undesirable since they may lead to minority charge storage, which complicates diode turn-off (forced diode reverse recovery) and may lead to snapback of the parasitic source-body-drain active cell NPN bipolar transistor when a high reverse voltage is once again applied across the device.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 illustrates a cross-sectional view of a conventional trench-gated MOSFET containing a deep central diffusion to reduce the electric field at the corners of the trenches.

Fig. 2A illustrates a cross-sectional view of a conventional trench-gated MOSFET without a deep central diffusion and wherein the trenches extend into the substrate.

Fig. 2B illustrates an equivalent circuit diagram for the MOSFET of Fig. 2A.

Fig. 3 illustrates a cross-sectional view of a first embodiment of this invention including a protective diffusion in an adjacent MOSFET cell.

Fig. 4A illustrates a cross-sectional view of a second embodiment of this invention including a protective diffusion in an adjacent MOSFET cell and wherein the trenches extend into the substrate.

Fig. 4B illustrates an equivalent circuit diagram for the MOSFET of Fig. 4A.

Fig. 5 illustrates a top view of a conventional MOSFET cell.

Fig. 6 illustrates a top view of a square-celled MOSFET in accordance with this invention.

Fig. 7 illustrates a detailed top view of the square-celled MOSFET of Fig. 6.

Fig. 8 illustrates a top view of a striped-cell MOSFET in accordance with this invention.

Fig. 9 illustrates another cross-sectional view of the second embodiment in accordance with this invention.

Fig. 10 illustrates a cross-sectional view of a third embodiment in accordance with this invention.

Fig. 11 illustrates a cross-sectional view of a fourth embodiment in accordance with this invention.

Fig. 12 illustrates a cross-sectional view of a fifth embodiment in accordance with this invention.

Figs. 13A and 13B illustrate cross-sectional and top views, respectively, of a sixth embodiment, which includes a wide protective cell.

Figs. 14A-14E illustrate the steps of a process of fabricating the MOSFET shown in Fig. 3.

DESCRIPTION OF THE INVENTION

A first embodiment of the invention is illustrated in Fig. 3. A trench-gated MOSFET 30 is formed in N-epitaxial layer 14, which is grown on the top surface of N+ substrate 13. A gate 31, formed in a trench 32, is separated from the sem-
5   iconductor material by an oxide layer 31A. A cell 35 of MOSFET 30 also includes a P-body region 33, a shallow P+ con-
tact region 33A, and an N+ source region 34. A metal layer 36 makes contact with and forms a short between P-body region 33 and N+ source region 34.

N+ substrate 13 serves as the drain of MOSFET 30 and may be contacted from the bottom. Alternatively, a sub-
merged N+ layer instead of the N+ substrate could be used as the drain, and the drain could be contacted from the top
10   side of the structure by means of, for example, an N+ sinker region and a top side contact.

In a neighboring cell 37 a protective deep P+ diffusion 38 is formed. Diffusion 38 forms a PN junction 39 with N-
epitaxial layer 14. Metal layer 36 contacts protective diffusion 38, and thus PN junction 39 represents a diode which is
connected in parallel with the channel of cell 35.

Protective diffusion 38 limits the strength of the electric field and resulting carrier formation near the corners of
15   trench 32 and thereby eliminates the need for a deep central diffusion in MOSFET cell 35. With no deep central P+ dif-
fusion, the dimensions of MOSFET cell 35 may be substantially reduced and the cell density of MOSFET 30 may be
significantly increased. For example, the width of each side of N+ source region 34 may be reduced to about i.0μm, and
the width of the contact between metal layer 36 and the P+ contact region for P-body 33 may be reduced to about
1.0μm, so that the total width between trenches 31 may be on the order of 3.5μm, although in practice the total width
20   between trenches 31 might be set at 5.0μm. This compares with a minimum width of about 8.0μm for a MOSFET cell
which contains a deep central diffusion (see Fig. 1).

Fig. 4A illustrates a MOSFET 40 which includes a MOSFET cell 41 similar to the cell shown in Fig. 2A. That is,
trenches 43 extend through the N-epitaxial layer 14 and into the N+ substrate 13, and cell 41 does not include a central
deep P+ diffusion. In an adjacent cell 42, a protective P+ diffusion 44 is formed, with the lower junction of diffusion 44
25   reaching the top surface of N+ substrate 13.

Fig. 4B illustrates an equivalent circuit for MOSFET 40. Since the corners of trench 43 are located in the N+ sub-
strate 13, which being heavily-doped cannot support a strong electric field, the problem of the electric field at the cor-
ners of the trenches is largely eliminated. Instead, the critical factor becomes the strength of the electric field between
the gate 45 and the N+ substrate 13, i.e., across the gate oxide layer 45A. This location is represented by a capacitor
30   C_{GD} in Fig. 4B. The PN junction between P-body region 22 and N-epitaxial layer 14 is represented by a diode D_{DB}, and
the PN junction between P+ diffusion 44 and N+ substrate 13 is represented by a diode $D_{P+/N+}$. As shown, both diode
D_{DB} and diode $D_{P+/N+}$ and connected in parallel with the channel of MOSFET cell 41.

Fig. 5 shows a top view of the conventional MOSFET 10 shown in Fig. 1. The protective deep P+ region 15 is
shown at the center of each square cell, surrounded by the N+ source region 12 and the gate 11. Four complete cells
35   are shown in Fig. 5.

Fig. 6 shows a top view of the MOSFET 30 shown in Fig. 3. A top view of MOSFET 40 shown in Fig. 4A would
appear similar. Because the protective P+ region at the center of each cell has been eliminated, the dimensions of the
cells have been reduced. The cells which contain the P+ diffusions (sometimes referred to as "diode cells") are also
shown. In Fig. 6, there is one diode cell for every eight active MOSFET cells (total of nine cells).
40   Fig. 7 shows a detailed top view of three of the cells shown in Fig. 6 (two active MOSFET cells and one diode cell).
In Fig. 7, Y_S represents the distance between the trenched gates and Y_G represents the cross-sectional width of the
trench (not to be confused with the gate width W). Assuming that there is one diode cell for every n total cells, the fol-
lowing equation gives the total area A of the n cells:

$$A = (Y_G + Y_S)^2 + (n - 1)(Y_G + Y_S)^2 = n(Y_G + Y_S)^2$$

Since n-1 of these cells are active MOSFET cells, the total gate width W in the n cells is equal to:

$$W = 4 Y_S (n - 1)$$

Accordingly, the area-to-width ratio A/W (a figure of merit indicating how effectively a gate width W is packed into
an area A) equals:

$$\frac{A}{W} = \frac{(Y_G + Y_S)^2}{4 Y_S} \cdot \frac{n}{n-1}$$

Thus the ratio A/W for a MOSFET which contains diode cells is increased by the factor n/(n - 1), as compared with
a conventional MOSFET with no diode cells. This "penalty" factor, which arises from the fact that the diode cells carry

no current, approaches unity as n increases. The penalty is counterbalanced by the increased total gate width (and hence current-carrying capacity) which is obtained by increasing the cell density of the device. Generally, n is determined by the frequency with which the MOSFET is expected to break down. Devices which are expected to break down more frequently will generally require a lower n, i.e., there must be a greater number of diode cells relative to the total number of cells. In the extreme case where every other cell is an inactive (i.e., diode) cell, N = 2 and n/n - 1 = 2, the efficiency benefits of this structure are somewhat limited. On the other hand, if only one of every 21 cells is a diode, for example, n = 21 and n/n -1 = 21/20, representing virtually no penalty for the diodes.

In conclusion, the regularly distributed inclusion of non-active deep P+ cells in a vertical trench FET provides a voltage clamping feature which limits the carrier generation rate and electric field at the corners or in the vicinity of the trench gate. The reliability and survivability of the device in the presence of electrical overstressing is thereby improved without limiting on-resistance or cell density. The deep P+ region need not extend to the trench edge but may be made smaller than its cell geometry if desired. The deep P+ region need not extend below the trench if the trench overlaps the N+ substrate, in which case a PIN diode may be formed between the deep P+ region and the N+ substrate (see Fig. 11). A graph showing the breakdown voltage of a PIN diode (such as diode D2 in Fig. 11) as a function of the doping concentration and width of the intermediate or "intrinsic" region is provided in S.M. Sze, <u>Physics of Semiconductor Devices</u>, Second Edition, John Wiley & Sons (1981), p. 105, Fig. 32, which is incorporated herein by reference.

Fig. 8 illustrates a top view of an alternative MOSFET in which the cells are in the form of stripes. In MOSFET 80, cells 81, 82, 83 and 84 are active MOSFET cells, and cell 85 is a diode cell which contains a protective P+ diffusion 86. Each of cells 81-84 contains a P+ contact region 87 and an N+ source region 88. Contact holes 89, two of which are shown in Fig. 8, are used to provide contact between a metal layer (not shown) and P+ region 87 and N+ source region 88 in MOSFET cells 81-84 and P+ region 86 in diode cell 85. Contact holes 89 may be arranged in a variety of patterns over cells 81-85. A contact hole 90 for making contact with gate 91 is also shown.

Another use of the P+ diode cell is to clamp the drain voltage so as to protect the gate oxide layer from overstress due to excessive electric fields between the gate and the N+ substrate. This situation arises particularly in embodiments where the trench gate extends into the substrate and the gate oxide layer at the bottom of the trench is therefore exposed to the entire voltage difference between the gate and substrate. Silicon dioxide is capable of withstanding a voltage equal to about 8 MV/cm. Using a safety factor of 50%, the industry generally considers the maximum voltage that may be applied across a gate oxide layer to be $X_{OX} \cdot 4MV/cm$, X_{OX} being the thickness of the gate oxide in centimeters. Accordingly, the breakdown voltage of the diode that is formed by the protective P+ diffusion should be no greater than $X_{OX} \cdot 4MV/cm$. For example, with an oxide layer having a thickness of 400 Å, the oxide layer will rupture at about 32V, and for reliable operation the maximum voltage should be limited to 16V

Figs. 9-11 illustrate cross-sectional views of several alternative embodiments in accordance with the invention. Fig. 9 shows a MOSFET 92 in which the trenches extend into the N+ substrate 13. A thin layer of N-epitaxial layer remains in the MOSFET cells 93, while in diode cell 94 the protective P+ diffusion reaches the top surface of N+ substrate 13. In the MOSFET 100 shown in Fig. 10, the P-body regions in the MOSFET cells 101 extend to the top surface of the N+ substrate 13, and none of the N- doped region of epitaxial layer 14 remains. In the MOSFET 110 shown in Fig. 11, a thin section of the epitaxial layer 14, doped P- or N-, remains in each of the MOSFET cells 111 and the diode cell 112.

In Figs. 9-11, diode D1 represents the PN junction within the MOSFET cells, diode D2 represents the PN junction in the protective diode cells, and a capacitor C1 represents the gate oxide layer abutted by the gate and the N+ substrate. In all three cases the relationship $BV_{D2} < 50\% \cdot BV_{C1}$ should hold, where BV_{D2} is the breakdown voltage of diode D2 and BV_{C1} is the breakdown voltage of capacitor C1. Also, the breakdown voltage of diode D2 is less than the breakdown voltage of diode D1 in each case.

MOSFET 120, shown in Fig. 12, appears to be similar to the conventional MOSFET shown in Fig. 2A. Diode D1 represents the PIN diode formed at the center of each MOSFET cell by the combination of the shallow P+ contact region, the P-body and the N+ substrate. In MOSFET 120 the breakdown voltage of PIN diode D1 is set at less than 50% of the breakdown voltage of capacitors C1, wherein the breakdown voltage of the capacitors is calculated on the basis of 8 MV/cm for the thickness of the gate oxide layer expressed in centimeters. As a result, in MOSFET 120 breakdown will occur, if at all, in the central region of the individual cells and at a voltage which will not damage the gate oxide layers.

Another alternative embodiment is illustrated in Figs. 13A and 13B, Fig. 13A being a cross-sectional view taken at section XIIIA-XIIIA shown in the top view of Fig. 13B. MOSFET 130 includes cells 121 as well as a wider cell 131 which includes a deep P+ region 132. Deep P+ region 132 provides a protective function for the gate oxide layers in cells 121 while acting as an active MOSFET cell itself, having an N+ source region 133. Thus, while cell 131 reduces the overall cell density of the MOSFET, the penalty in terms of on-resistance is less than it would be if cell 131 performed only a protective function and carried no current. As in MOSFET 120 of Fig. 12, cells 121 are typically smaller than they would be if a protective deep P+ region were included in each cell.

Although there are numerous processes for fabricating a MOSFET in accordance with this invention, Figs. 14A-14E illustrate an exemplary process for fabricating MOSFET 30 shown in Fig. 3.

Referring to Fig. 14A, the starting point is a conventional N+ substrate 13 on which an N-epitaxial layer 14 is grown using known processes.

A thick oxide layer 130 is grown, masked and etched, and a thin oxide layer 131 is grown on the top surface of the structure where deep P+ region 38 is to be formed. Deep P+ region 38 is then implanted through thin oxide layer 131
5   at a dose of 1×10^{14} to 7×10^{15} cm^{-2} and an energy of 60-100 keV. The resulting structure is illustrated in Fig. 14A. Oxide layers 130 and 131 are then removed.

In one version of the process, a thick oxide layer 132 is grown and removed by photomasking except over deep P+ region 38, and a thin oxide layer 133 is grown. Thin oxide layer 133 is masked and removed from the portions of the structure where the trenches are to be formed, as shown in Fig. 14B. The trenches are then masked and etched using
10   known techniques of reactive ion or plasma dry etching. Then the trench is oxidized to form gate oxide layer 31A, and polysilicon is deposited into the trench until it overflows the top of the trench. The polysilicon is then doped with phosphorus by POCl$_3$ predeposition or ion implantation at a dose of 5×10^{13} to 5×10^{15} cm^{-2} and an energy of 60 keV, giving it a sheet resistance of 20-70 Ω/□. For a P-channel device, the polysilicon is doped with boron using ion implantation to a sheet resistance of roughly 40-120 Ω/□. The polysilicon is then etched back until it is planar with the surface of the
15   trench except where a mask protects it, so that it can subsequently be contacted with metal.

P-body 33 is then implanted through the thin oxide layer 133 (e.g., boron at a dose of 1×10^{13} to 4×10^{14} cm^{-2} and an energy of 40-100 keV). A similar method is used in fabricating a P-channel device except that the dopant is phosphorus. The resulting structure is illustrated in Fig. 14C.

The N+ source region 34 is then introduced using a mask and an arsenic ion implantation (or a boron ion implan-
20   tation for a P-channel device) at a dose of 5×10^{14} to 1×10^{16} cm^{-2} at 20 to 100 keV. The resulting structure is shown in Fig. 14D.

Following the formation of the N+ source region 38, a new mask is formed and the shallow P+ region 33A that is used to contact the P-body is introduced by ion implantation at a dose of 1×10^{13} to 5×10^{14} cm^{-2} at 20-80 keV. Alternatively, as shown in Fig. 14E, shallow P+ region 33A can be formed by implanting P-type dopant through the same
25   mask that is used in forming the contact holes for the N+ source region/P+ contact region and the deep P+ region. Although with this technique some of the P-type dopant is implanted into N+ source region 34, the level of P-type doping is not sufficient to significantly affect the concentration of N-type ions in the N+ source region.

A thin oxide layer is thermally grown. Borophosphosilicate glass (BPSG) is then deposited on the surface of the structure. The BPSG is momentarily heated to around 850° to 950°C to flow smoothly and flatten the surface topology
30   of the die. Contact holes are etched in the oxide and BPSG layers, and metal layer 36 is deposited, forming contacts with the source and body regions and the deep P+ region through the contact holes. This yields MOSFET 30 shown in Fig. 3.

The die is then passivated with SiN or BPSG, and pad mask windows are etched to facilitate bonding.

The embodiments described above are illustrative only and not limiting. Numerous alternative embodiments in
35   accordance with the broad principles of this invention will be apparent to those skilled in the art.

Claims

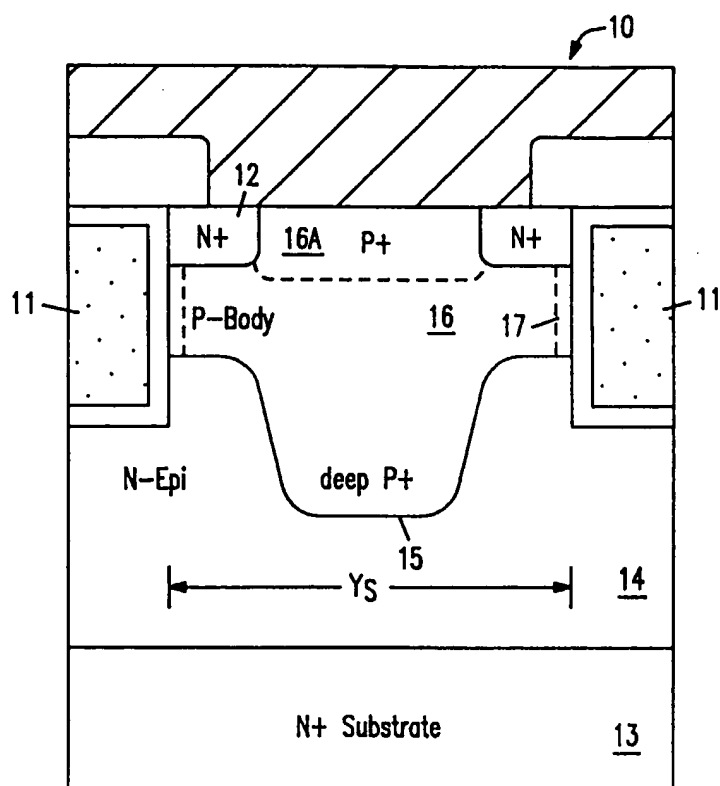1. A trench-gated power MOSFET comprising:

40

    a semiconductor material;
    a gate positioned in a trench formed in a surface of said semiconductor material, said trench defining a plurality of MOSFET cells, each of said MOSFET cells comprising a source region of a first conductivity type and a body region of a second conductivity type adjoining said source region, said source region and said body region
45   abutting a side of said trench;
    a protective diffusion of said second conductivity type, said protective diffusion adjoining a region of said first conductivity type so as to form a diode, said diode being connected in parallel with a channel region in each of said MOSFET cells.

50 2. The MOSFET of Claim 1 wherein said trench defines a diode cell, said protective diffusion being located in said diode cell.

3. The MOSFET of Claim 2 wherein said semiconductor material comprises a substrate and an epitaxial layer formed on a surface of said substrate.

55

4. The MOSFET of Claim 3 wherein a bottom of said trench is located in said epitaxial layer and is separated from an interface between said substrate and said epitaxial layer.

5. The MOSFET of Claim 4 wherein a bottom of said protective diffusion is located in said epitaxial layer and is separated from an interface between said substrate and said epitaxial layer.

6. The MOSFET of Claim 5 wherein said protective diffusion is shorted to the source region of each of said MOSFET cells.

7. The MOSFET of Claim 2 comprising a plurality of said diode cells, said diode cells being positioned at regular intervals in a lattice formed by said gate.

8. The MOSFET of Claim 7 wherein there are a predetermined number of said MOSFET cells for every diode cell.

9. The MOSFET of Claim 3 wherein a bottom of said trench is located in said substrate.

10. The MOSFET of Claim 9 wherein a bottom of said protective diffusion is located at an interface between said substrate and said epitaxial layer.

11. The MOSFET of Claim 9 wherein a region of said first conductivity in said epitaxial layer separates said body region from said substrate in said MOSFET cells.

12. The MOSFET of Claim 2 wherein said trench forms a lattice of square cells.

13. The MOSFET of Claim 2 wherein said trench forms a lattice of cells in the form of stripes.

14. The MOSFET of Claim 9 wherein said gate is separated from said semiconductor material by a gate oxide layer, and wherein said diode has a breakdown voltage that is lower than a voltage that causes damage to said gate oxide layer.

15. The MOSFET of Claim 11 wherein a region of said first conductivity in said epitaxial layer separates said protective diffusion from said substrate in said diode cell.

16. A trench-gated power MOSFET comprising:

a semiconductor material comprising a substrate and an epitaxial layer formed on a surface of said substrate; a gate positioned in a trench and separated from said semiconductor material by an oxide layer, said trench being formed in a surface of said epitaxial layer and extending into said substrate, said trench defining a plurality of MOSFET cells, each of said MOSFET cells comprising a source region of a first conductivity type and a body region of a second conductivity type adjoining said source region, said source region and said body region abutting a side of said trench; wherein said body region adjoins a drain region of said first conductivity type, a PN junction between said body region and said drain region forming a diode, and wherein said diode has a breakdown voltage that is lower than a voltage that causes damage to said oxide layer.

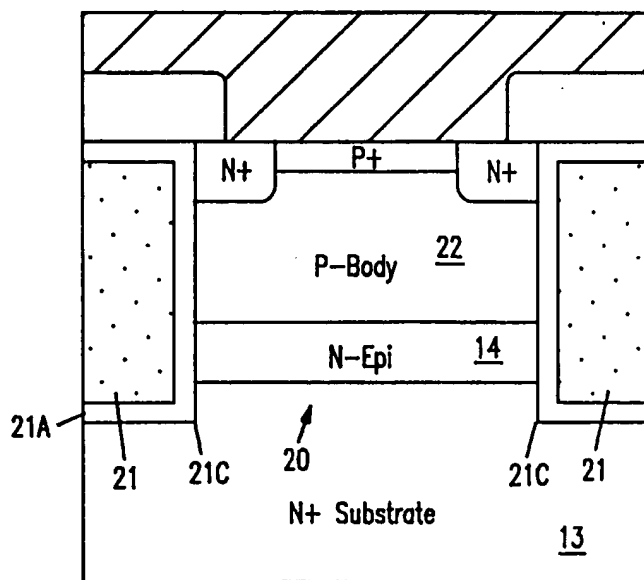17. The MOSFET of Claim 16 wherein said body region is shorted to said source region in each of said MOSFET cells.
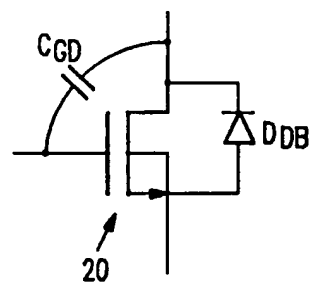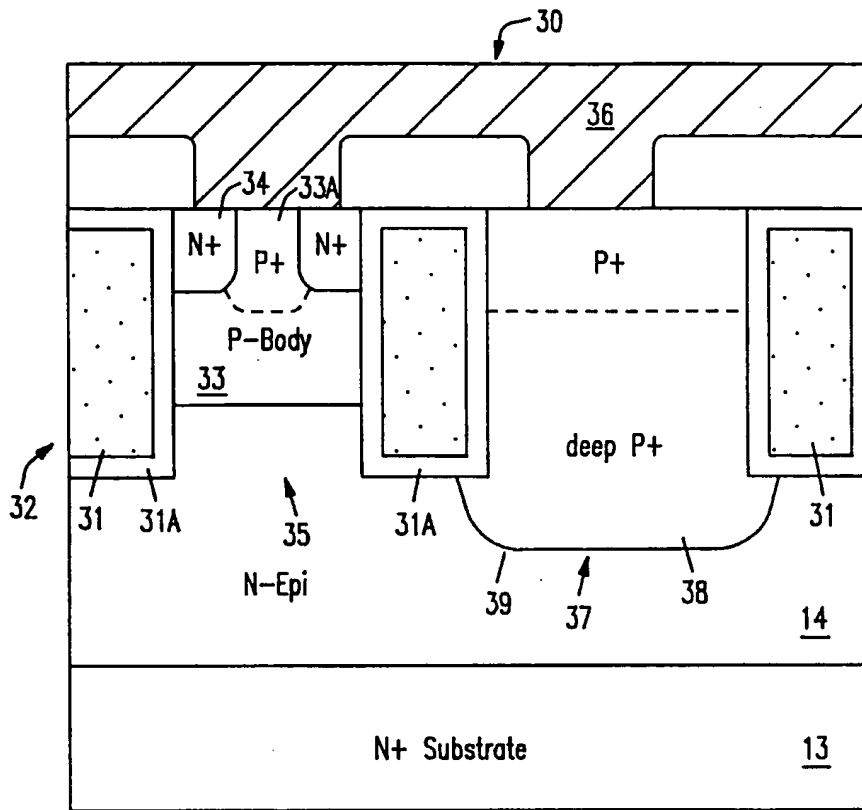
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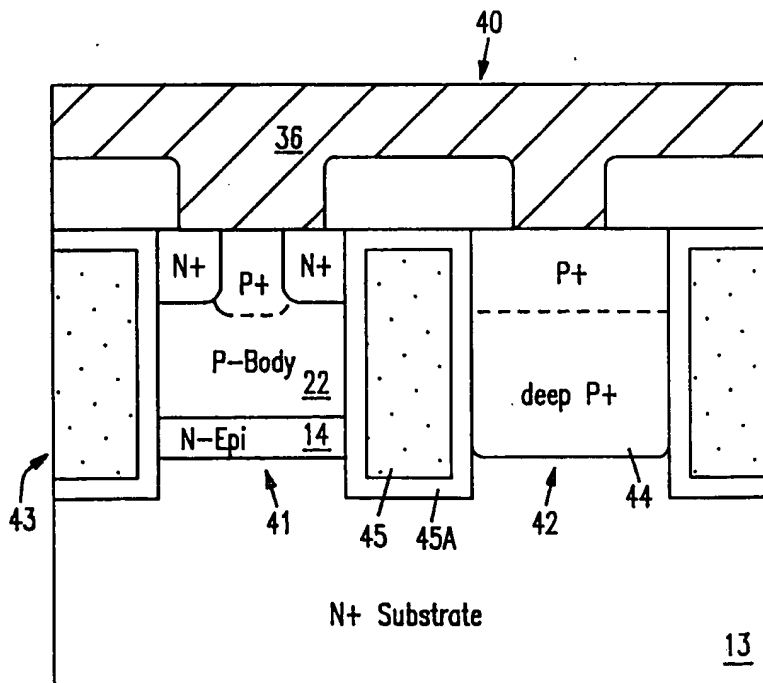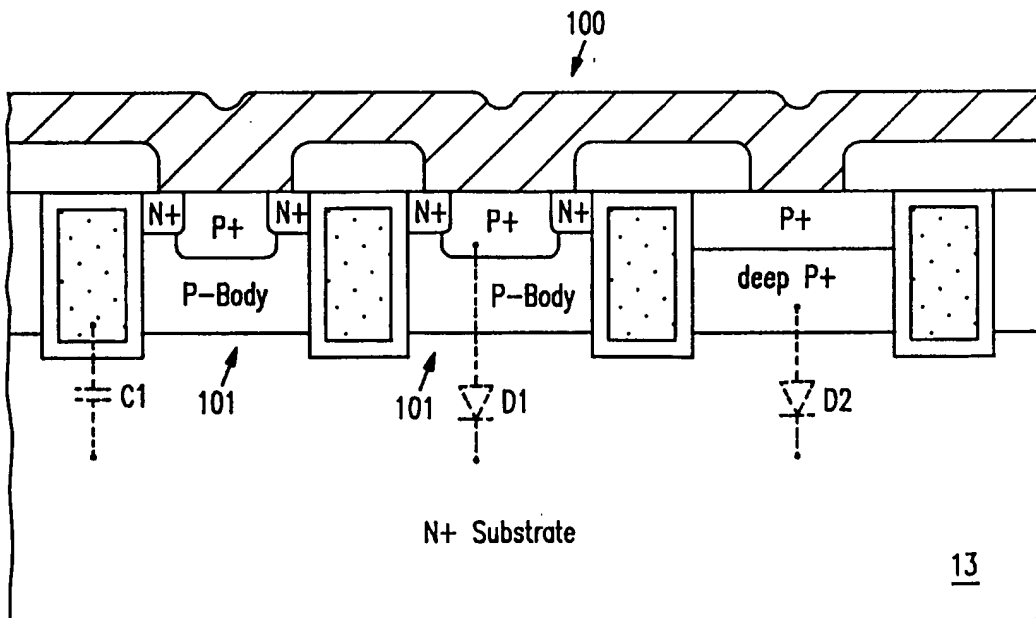FIG. 1

FIG. 2A

FIG. 2B

FIG. 3

FIG. 4A

C_{GD}

D_{DB} $D_{P+/N+}$

FIG. 4B

12

15

11   P+   N+   P+   N+

Trench

P+   N+   P+   N+

FIG. 5

P+   P+

Trench

FIG. 6

FIG. 7

FIG. 8

92

N+	P+	N+	N+	P+	N+	P+

P–Body   P–Body

N–Epi   N–Epi   14   deep P+

C1   93   93   D1   D2

N+ Substrate

13

FIG. 9

100

N+	P+	N+	N+	P+	N+	P+

P–Body   P–Body

deep P+

C1   101   101   D1   D2

N+ Substrate

13

FIG. 10

110

N+ | P+ | N+ | N+ | P+ | N+ | P+

P—Body | P—Body | P—Body

P or N—Epi | P or N—Epi | P or N—Epi

C1 | 111 | 111 | D1 | 112 | D2

N+ Substrate

FIG. 11

120

N+ | P+ | N+ | N+ | P+ | N+ | N+ | P+ | N+

P—Body | P—Body | P—Body

C1 | 121 | 121 | 121 | D1

N+ Substrate

$BV_{D1} < BV_{C1}$

FIG. 12

FIG. 13A

FIG. 13B

130   P↓   131

P+

38

N-Epi   14

N+ Substrate   13

FIG. 14A

133   132

P+

38

N-Epi   14

N+ Substrate   13
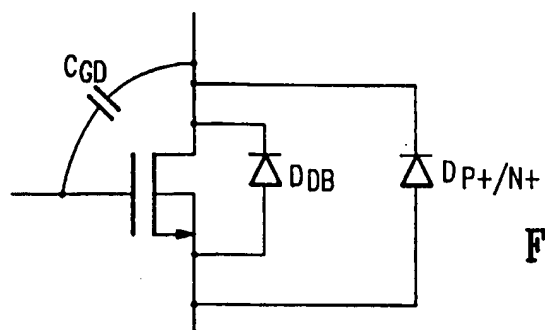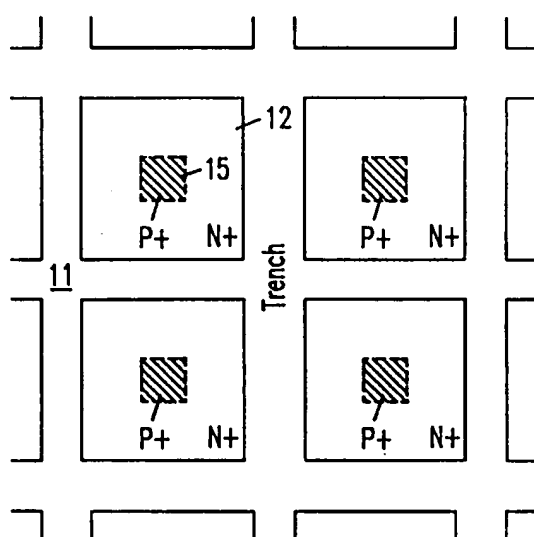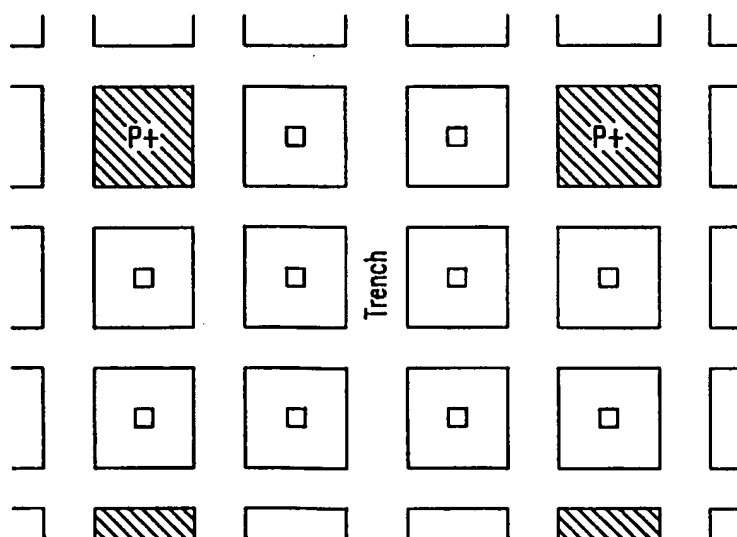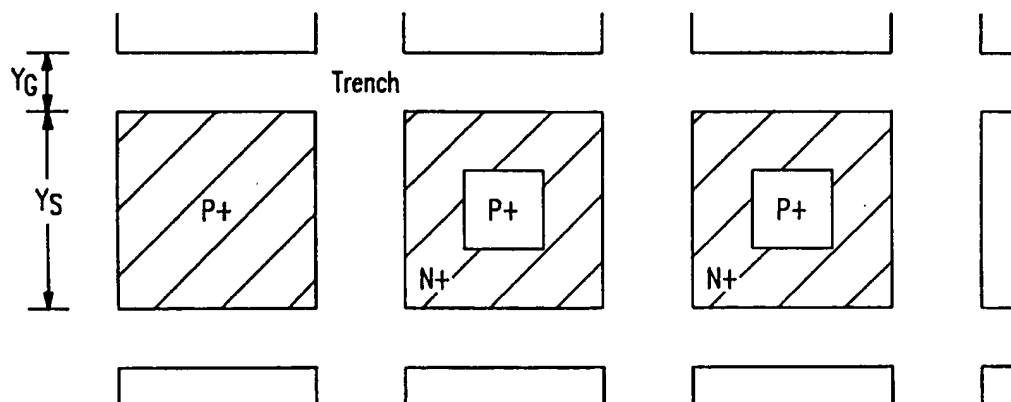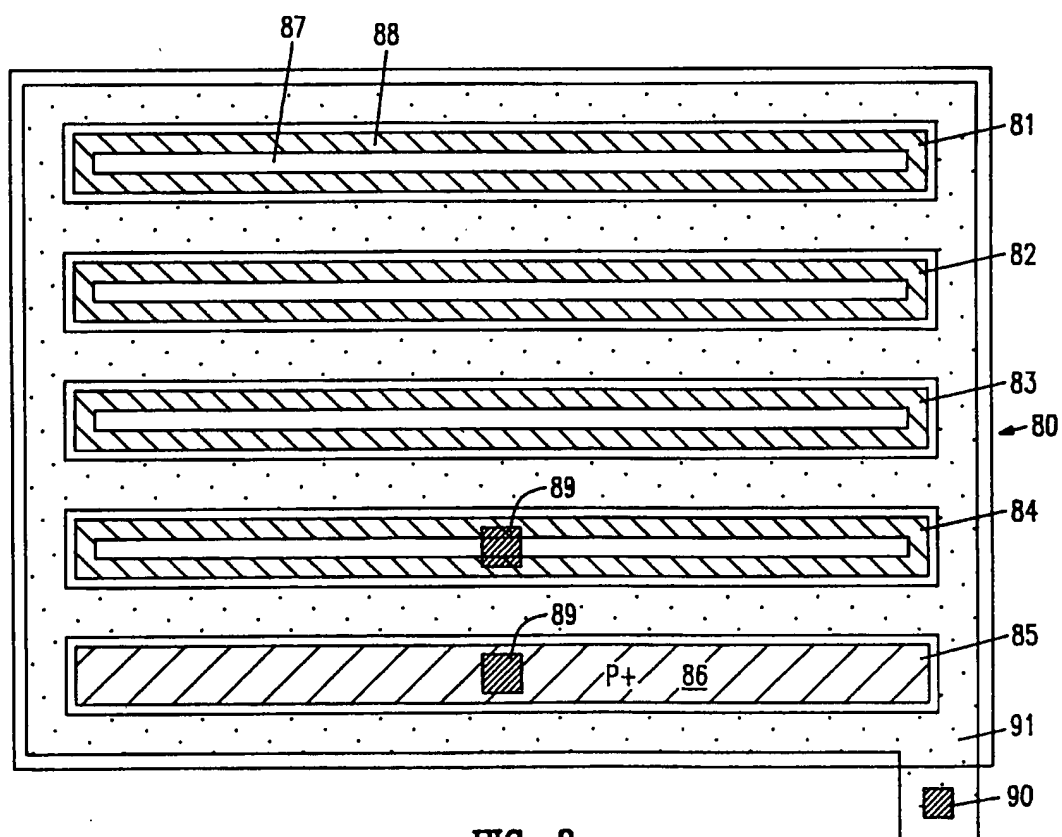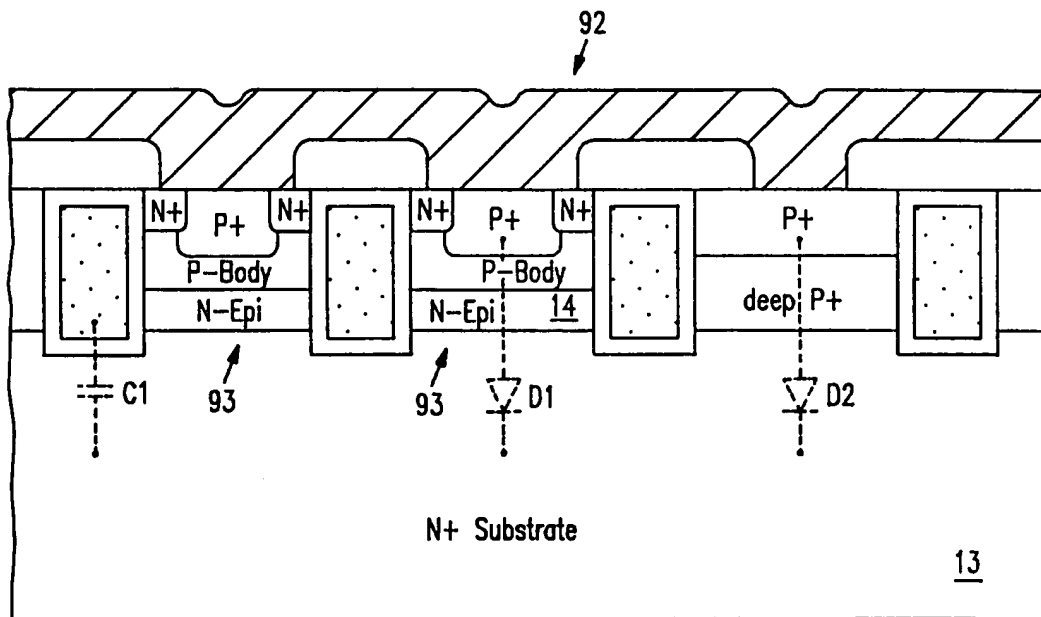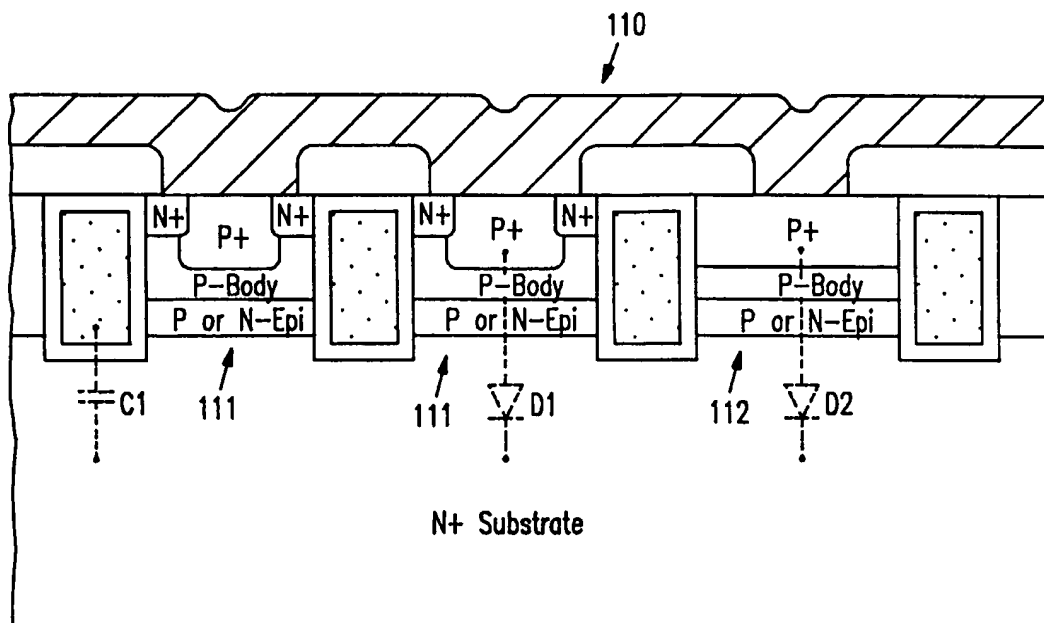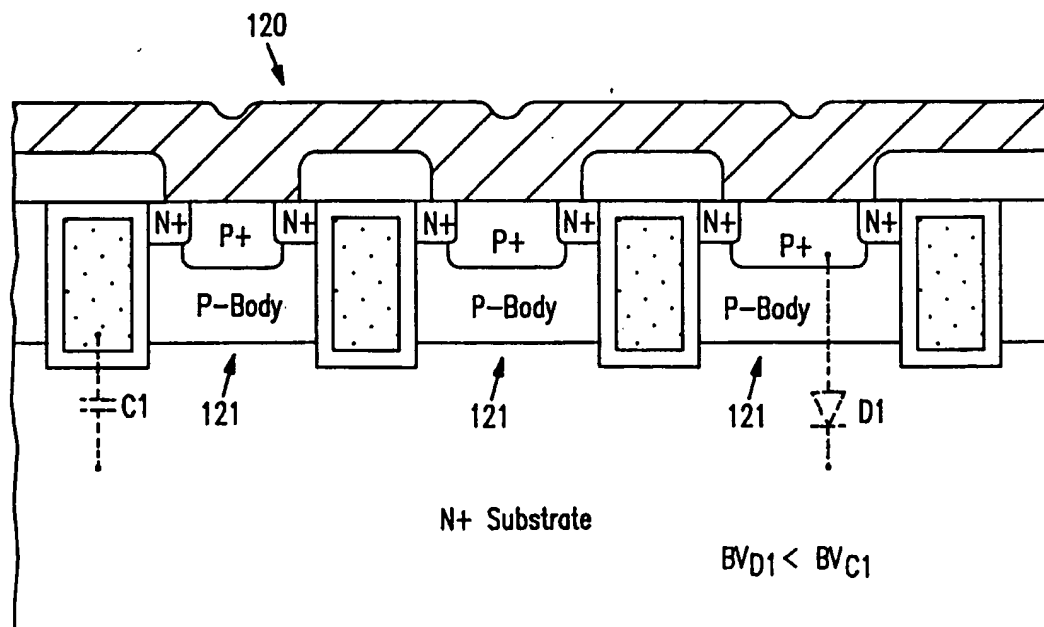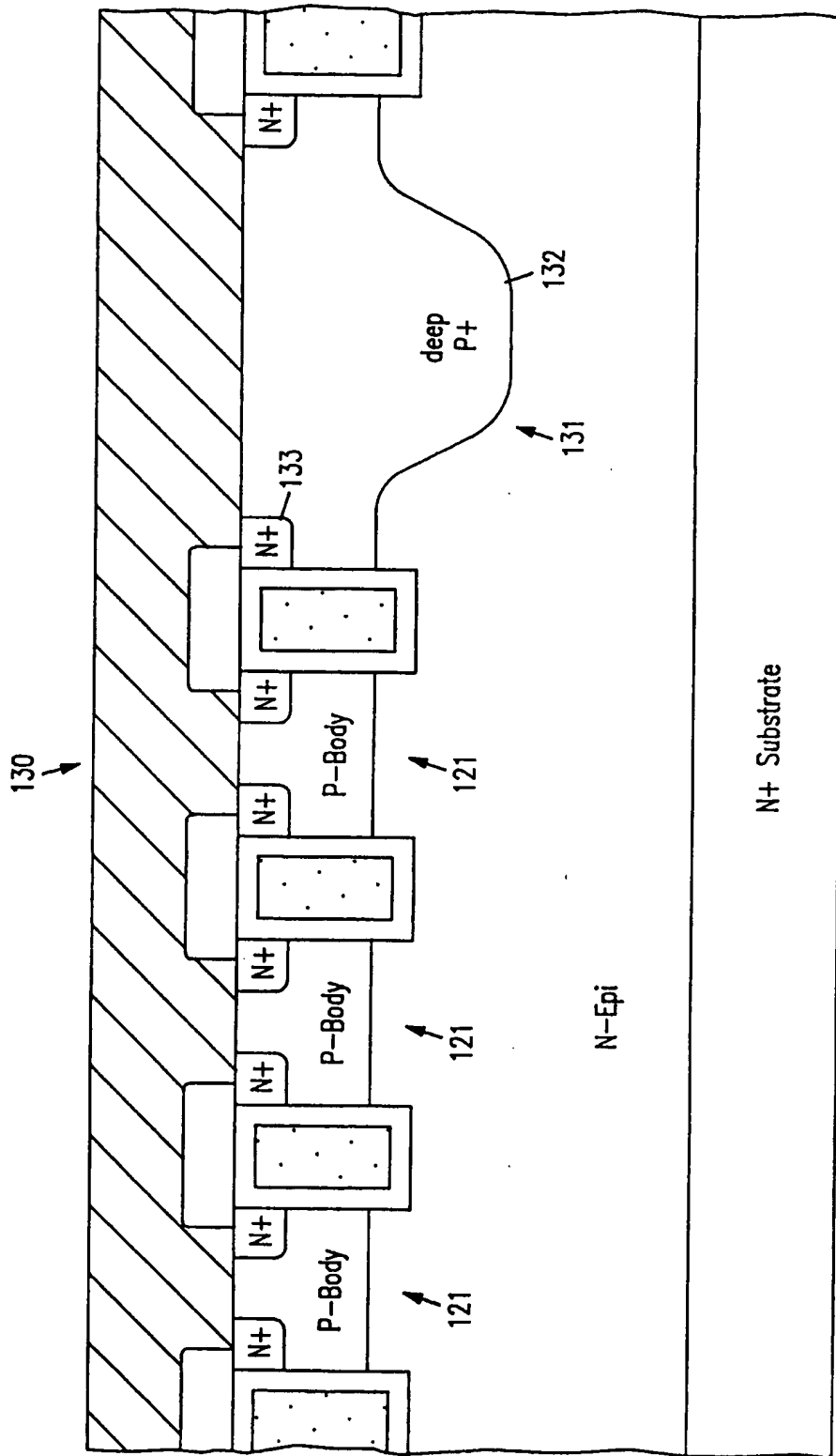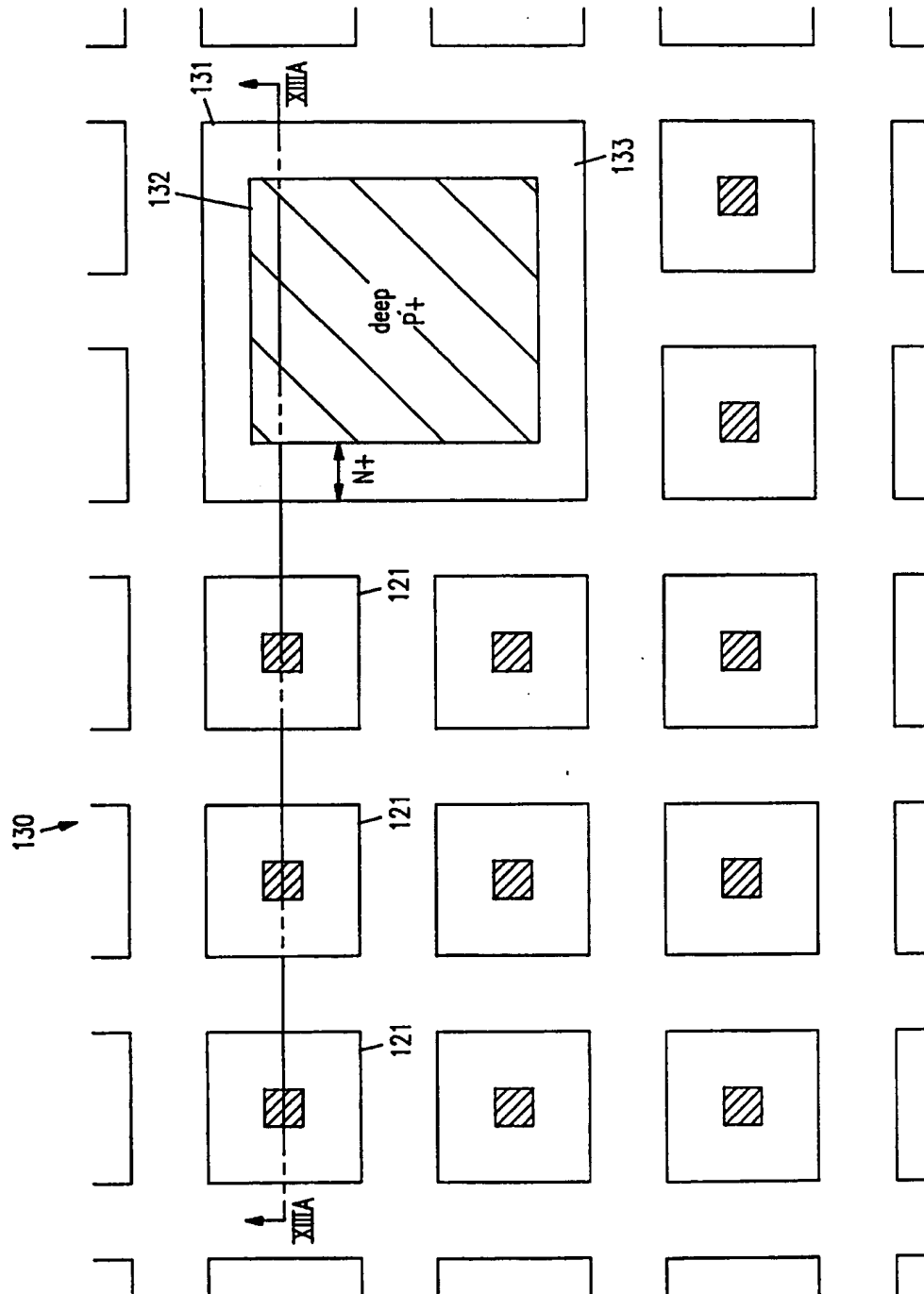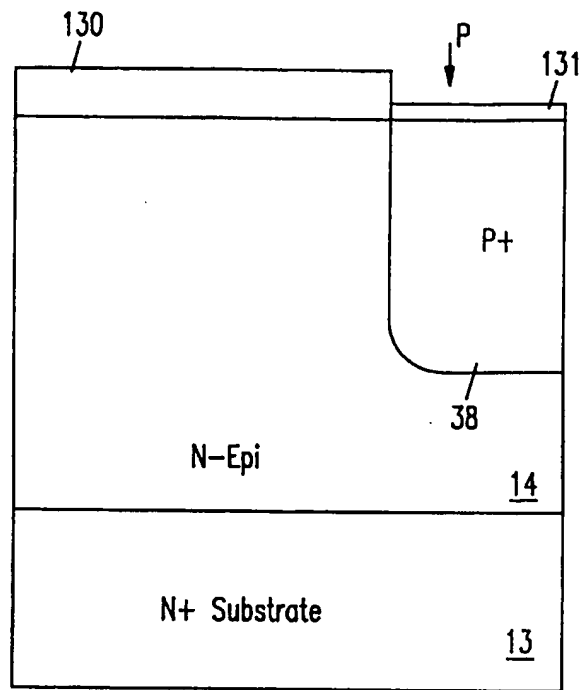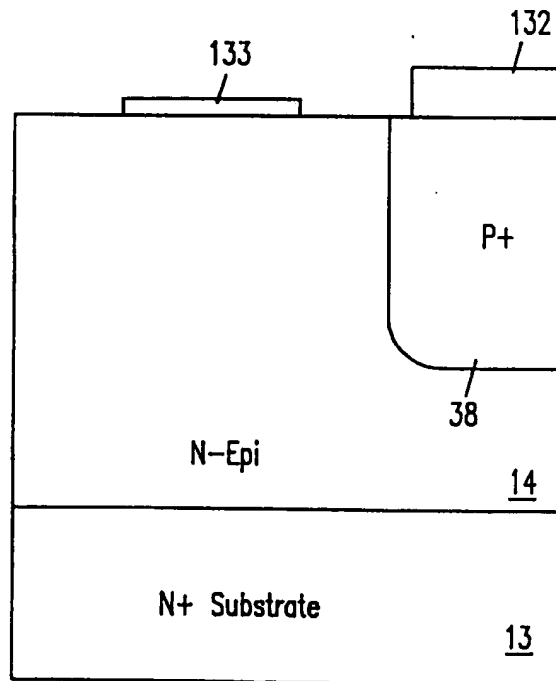
FIG. 14B

FIG. 14C

FIG. 14D

FIG. 14E